REMARKS

Prior to the present response, claims 22, 25 and 28 were pending in the present application. No claims are amended by the present response. Thus, claims 22, 25 and 28 remain in the present application. Reconsideration and allowance of pending claims 22, 25 and 28 in view of the following remarks are respectfully requested.

A. Rejections of Claims 22, 25 and 28 under 35 USC § 102(b)

The Non-Final Office Action dated April 6, 2010 (hereinafter "Office Action") rejects claims 22, 25 and 28 under 35 U.S.C. § 102(b) for purported anticipation by U.S. Patent Application Publication Number 2004/0002185 by Takahashi et al. (hereinafter "Takahashi"). *See* item 3 of the Office Action. For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by previously presented independent claims 22, 25 and 28, is patentably novel and inventive over Takahashi.

The present invention, as defined by independent claims 22, 25 and 28, is directed to a field effect transistor (FET) having increased carrier mobility due to tensile strain in the FET's channel. As explained in the present application, the tensile strain in the FET's channel is purposefully caused by forming, at a high wafer temperature, a first gate dielectric having a first coefficient of thermal expansion (CTE) over the channel, forming a second gate electrode having a third CTE over the first gate dielectric, and forming a first gate electrode having a second CTE over the second gate electrode, where the third CTE is larger than the first CTE and less than the second CTE. *See*, e.g.,

page 7 line 18 through page 9 line 7 with Figure 2 of the present application. By forming both electrodes at high wafer temperatures, the resulting structure causes a tensile strain in the FET's channel that, in turn, causes the desired increased carrier mobility. *Id.* Independent claims 22, 25 and 28 emphasize the present invention's structure configuration causing the advantageous increase in carrier mobility by reciting a second gate electrode situated between said first gate electrode and said first gate dielectric, said second gate electrode having a third coefficient of thermal expansion, said third coefficient of thermal expansion being greater than said first coefficient of thermal expansion and said third coefficient of thermal expansion being less than said second coefficient of thermal expansion so as to cause a tensile strain in said channel, said tensile strain causing said increase in said carrier mobility.

By contrast to the present invention, Takahashi is directed to manufacturing a dual-gate complementary metal on oxide field effect transistor (CMOSFET), and seeks to solve problems in simultaneous P and N MOS gate stack fabrication, such as undesirable dopant or impurity migration during gate stack formation. See paragraphs [0013] through [0021] of Takahashi. Nowhere does Takahashi disclose or suggest introducing strain into its CMOSFET structure to increase carrier mobility, as is required by independent claims 22, 25 and 28, as explained above. Instead, Takahashi teaches performing multiple annealing steps at temperatures exceeding 900 degrees C throughout it's method, including an annealing step at 1000 degrees C used to activate its polycrystalline silicon layer 22. *See id.*, at paragraphs [0058] and [0061]. As is known in the art, an annealing process performed on a semiconductor structure

experiencing mechanical strain due to CTE mismatch can reduce or eliminate that strain. *See*, e.g., Kahn et al, *Thermal Expansion of Low-Pressure Chemical Vapor Deposition Polysilicon Films*, Abstract, Journal of Materials Research, vol. 17, issue 7, pp. 1855-1862 (provided herein as evidence only). Thus, not only does Takahashi fail to disclose the present invention, Takahashi actively teaches away from forming tensile stress in a semiconductor structure, as required by independent claims 22, 25 and 28, by requiring multiple high-temperature annealing processes to enable its method.

The Office Action attempts to sidestep this deficiency of Takahashi by noting that Takahashi's structure includes silicon dioxide as a first gate dielectric, polysilicon as a second gate electrode, and WSi as a first gate dielectric, and then arguing, by citing to further art references as support, that the materials' CTEs meet the requirements of and thus anticipating the present invention, as defined by independent claims 22, 25 and 28. *See* page 3 of the Office Action. Applicants respectfully disagree. First, Applicants point out that the Office Action is apparently comparing linear CTEs against a volumetric CTE, and thus the comparison of the relative CTEs is per se invalid. *See* Table 1 of U.S. Patent No. 5,557,136 to Gordon et al.; *and see* column 2 lines 40-42 of U.S. Patent No. 6,864,556 to You et al. Second, even if Takahashi's first gate dielectric, second gate electrode, and first gate electrode had increasing CTEs, nowhere does Takahashi disclose or suggest forming the electrodes at high temperatures so that the increasing CTEs cause a tensile strain in a channel of its CMOSFET, as is required by the present invention and independent claims 22, 25 and 28. Thus, Applicants

respectfully submit that Takahashi fails to disclose or even suggest the present invention, as defined by independent claims 22, 25 and 28.

For the foregoing reasons, Applicants respectfully submit that at the time the invention defined by previously presented independent claims 22, 25 and 28 was made, the invention was not anticipated by, nor would have been obvious in light of the disclosure provided by Takahashi. Thus, Applicants respectfully submit that previously presented independent claims 22, 25 and 28 are patentably novel and inventive over Takahashi.

B. Conclusion

Based on the foregoing reasons, Applicants respectfully submit that the present invention, as defined by previously presented independent claims 22, 25 and 28 is patentably novel and inventive. Moreover, Applicants assert that no new matter has been introduced herein. Thus, for all of the reasons presented above, early allowance of claims 22, 25 and 28 pending in the present application is respectfully requested.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

Attorney Docket No.: 0180144

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 9/7/10

Michael Farjami, Esq.
Reg. No. 38,135

FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Telephone: (949) 282-1000
Facsimile: (949) 282-1002

CERTIFICATE OF FACSIMILE TRANSMISSION
I hereby certify that this correspondence is being filed by facsimile transmission to United States Patent and Trademark Office at facsimile number **(571) 273-8300** on the date stated below. The facsimile transmission report indicated that the facsimile transmission was successful.

Date of Facsimile: 9/7/10

Jembier Davalos
Name of Person Performing Facsimile Transmission

Jembier Davalos 9/7/10
Signature Date

H1867